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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,804	02/25/2005	Johannes Petrus Maria Van Lammeren	NL02 0783 US	1168

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EXAMINER	
MARSH, OLIVIA MARIE	
ART UNIT	PAPER NUMBER
2617	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/525,804	VAN LAMMEREN ET AL.	
	Examiner	Art Unit	
	Olivia Marsh	2617	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-13* is/are rejected.

7)☒ Claim(s) *8,9,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/25/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a) merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte*

Hasche, 86 USPQ 481 (Bd. App. 1949). In the present instance, line 3 recites the broad recitation "sub-circuit", and the claim also recites "first and second sub-circuit" which is the narrower statement of the range/limitation.

For the purposes of apply prior art, the Examiner will assume Applicant meant the "sub-circuit" limitation provided in line 3 to read as "first sub-circuit."

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7 and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Easter *et al* (U.S. 5,530,749 A).

As to **claim 1**, Easter discloses:

> A circuit module **(FIG 3, 210)** comprising a first **(104, 214)** and second sub-circuit **(100, 216)** and a communication link coupled between the first and the second sub-circuit, the sub-circuits being arranged to communicate signals via the communication link during operation **(column 4, lines 1-15; FIG 6.; column 6, lines 59-67; column 7, lines 1-3)**;
>
> the sub-circuit **(104, 214)** comprising a version number memory **(106)** for storing a version number, the sub-circuit providing a performance dependent on the version number that is stored in the version number memory **(column 4,**

lines 13-15; column 5, lines 5-7; column 6, lines 44-47; column 7, lines 18-20);

the second sub-circuit **(100, 216)** comprising a write-protected memory **(100, 216)** and a version number control circuit **(102)** arranged to send update values for the version number memory from the write-protected memory via the communication connection **(column 4, lines 12-15, 54-57; column 5, lines 5-7; column 6, lines 66-67; column 7, lines 15-20)**.

As to **claim 2**, Easter discloses everything as applied in claim 1 above and Easter also discloses:

the circuit module is a multi- component module, comprising a package that contains the first sub-circuit in a first integrated circuit and the second sub-circuit in a second integrated circuit **(FIGs 3 and 6)**.

As to **claim 3**, Easter discloses everything as applied in claim 1 above and Easter also discloses:

the control circuit is arranged to send the update values multiplexed with normal operating signals that are communicated between the first and the second sub-circuit **(column 7, lines 10-20)**.

As to **claim 4**, Easter discloses everything as applied in claims 1 and 3 above and Easter also discloses:

the communication connection is a communication bus coupled to the sub-circuits, the first sub-circuit being arranged to support execution of commands received via the communication bus, including an update command for updating the version number in the version number memory **(column 6, lines 59-62)**; the circuit module comprising:

an external bus input **(column 6, line 61)**;

the version number control circuit being a watchdog circuit coupled between the external bus input and the communication bus, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus conditionally, the watchdog circuit detecting whether the update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write protected memory **(column 7, lines 5-22)**.

As to **claim 5**, Easter discloses everything as applied in claims 1 and 3-4 above and Easter also discloses:

comprising a processor integrated circuit containing a CPU **(engine 212)** and the write-protected memory, the first sub-circuit being a signal processing unit distinct from the processor integrated circuit, the CPU being arranged to provide a performance dependent on the version number that is stored in the write-protected memory **(column 6, lines 66-67; column 7, lines 1-3)**.

As to **claim 6**, Easter discloses everything as applied in claims 1 and 3-5 above and Easter also discloses:

the watchdog circuit comprises a register, the circuit module being arranged to write a copy of the version number from the write-protected memory in the register on power up, the watchdog circuit replacing the version number in the command by the version number from the register **(column 5, lines 18-21)**.

As to **claim 10**, Easter discloses:

A processor integrated circuit **(210, FIG 6)** comprising:

a write-protected memory **(100, 216)**;

operating circuits arranged to provide a performance dependent on a version number that is stored in the write-protected memory **(218-234)**;

an external bus input **(200, 202)**;

a communication bus output **(outputs to 218-234; FIG 6)**;

a watchdog circuit **(214)** coupled between the external bus input and the communication bus output, the watchdog circuit being arranged to pass commands from the external bus input to the communication bus output conditionally, the watchdog circuit detecting whether an update command to update the version number is received and if so to pass said update command, replacing a version number in the update command by a version number from the write-protected memory **(column 6, lines 59-67; column 7, lines 1-22)**.

As to **claim 11**, Easter discloses:

A signal processing circuit **(210)** comprising:

a version number memory for storing a version number **(215)**;

operating circuits **(218-234)** arranged to provide a signal processing with a performance dependent on a version number that is stored in the write-protected memory **(216)**;

an input and/or output for receiving and/or transmitting input signal to be processed or results of signal processing by said operating circuits **(200, 202, output lines 218-234; FIG 6)**;

a control circuit **(214)** arranged to detect multiplexed data in a predetermined format of the input signal or result and to cause data from the input and/or output that is received during said time slot to be copied to the version memory **(column 6, lines 59-67; column 7, lines 1-22)**.

As to **claim 12**, Easter discloses:

A method of controlling operation of a circuit module **(FIG 3, 210, column 3, lines 65-67; column 6, lines 44-47)**, the method comprising

providing a performance level of a first sub-circuit **(104, 214)** dependent on the version number that is stored in a version number memory **(column 4, lines 13-15, 51-52, 59-60; column 7, lines 1-3)**;

passing a version number from a write-protected memory **(100, 216)** from a second sub-circuit **(100, 216)** of the circuit module to the version memory multiplexed with normal operating signals for the first sub-circuit **(column 5, lines 2-7, column 7, lines 6-22)**.

As to **claim 13**, Easter discloses everything as applied in claim 12 above and Easter also discloses:

receiving commands for the circuit module and distributing the commands to the first sub-circuit via a communication bus **(FIG 6, column 6, lines 61-65)**;

monitoring received commands for an update command that commands updating of the version number in the version number memory and if so to pass said update command to the communication bus, replacing a version number in the update command by a version number from the write-protected memory **(column 7, lines 1-22)**.

Allowable Subject Matter

7. Claims 8-9 and 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Olivia Marsh whose telephone number is 571-272-7912. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nick Corsaro can be reached on 571-272-7876. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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